



High Performance Computing Software

JPL Internal Seminar Series

PIM Lite: A Multi-threaded Processor-in-Memory Chip for Massively-Parallel Computing

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JPL, Building 126, Room 225

Processing In Memory (PIM) technology (mixing significant processing logic with dense memory on the same chip) has become a popular new emerging trend in recent years. In many cases, however, it has been used simply as a step towards a "system on a chip," and as such has not engendered many new execution model or architectural ideas. In contrast, current research at the University of Notre Dame and Caltech assumes that PIM systems will be inherently massively parallel, with large numbers of relatively light weight threads executing within the PIM nodes. To take advantage of these characteristics, researchers at Notre Dame have designed a new ISA and matching micro architecture that supports such multithreading in ways that exploits the expanded local bandwidth and reduced latency capable from an on chip memory macro. A prototype VLSI implementation of this architecture, named PIM Lite, is about to go to fab as a memory part with multiple internal nodes, all of which support very light weight threads in a simple SMT micro architecture. This talk will discuss PIM Lite, and then our outlook on what more advanced designs might look like.

For questions, please contact Hans Zima at 354-8980.